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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2]  
3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [ Apr 3th, 2024

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### **Timer NE/SA/SE555/SE555C - 555 Timer Circuits**

Timer NE/SA/SE555/SE555C August 31, 1994 346 853-0036 13721 DESCRIPTION  
The 555 Monolithic Timing Circuit Is A Highly Stable Controller Capable Of Producing Accurate Time Delays, Or Oscillation. In The Time Delay Mode Of Operation, The Time Is Precisely Controlled By One External Resistor And Capacitor. For A Stable Operation As An Oscillator , The Jan 2th, 2024

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Keyless Entry Remotely Locks And Unlocks Your Power Door Locks. May 4th, 2024

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